REMARKS/ARGUMENTS

Prior to this Amendment, claims 1-16, 18, 19, and 25-30 were pending in this application.

Claim 1 is amended to clarify that a peripheral-share register resides at and is associated with each peripheral device in the embedded computer system. In each of these registers, a state value that is used by the multiplexor to determine which processor can be coupled with each peripheral. Claim 13 is likewise amended to clarify the association of the peripheral-share register with the peripherals. Similarly, independent claim 25 is amended to clarify that a peripheral register is associated with each of the peripheral units. Dependent claim 26 is canceled. No new matter is added with support being found at least in Figure 2 and paras. [0029] and [0030].

Claims 9-12 are canceled.

Claims 1-8, 13-16, 18, 19, 25, and 27-30 remain in the application for consideration by the Examiner. The amendments place the claims in condition for allowance or in better condition for use on appeal, and Applicants respectfully request that the amendments be entered and fully considered by the Examiner.

Rejection under 35 U.S.C. 103 of Claims 1-2, 5, 7-8, and 25-28

In the final Office Action of October 4, 2004, the rejection of claims 1-2, 5, 7-8, and 25-28 under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,408,671 ("Tanaka") in view of U.S. Pat. No. 5,408,627 ("Stirk") and further in view of U.S. Pat. No. 5,889,947 ("Starke") was maintained. This rejection is respectfully traversed based on the following remarks.

Claim 1 is amended to clarify that in the claimed embedded computer system that each of the peripheral-share registers is associated with a particular one of the peripherals and resides at that peripheral. An example of such an arrangement is shown in Applicants' Figure 2, which can be construed with Figure 1. As shown, a control register (i.e., peripheral-share register) 203 is provided for each peripheral and is shown to reside at or proximal to that peripheral. This one-to-one configuration of registers and peripherals and its

physical arrangement are not shown or suggested by any of the references of record.

Tanaka in Figure 1 and elsewhere shows processors coupled to shared memory registers and provides no teaching of peripheral-share registers residing at and being associated with each of a set peripherals. Stirk in Figures 3A, 3B, and 4 shows multiplexors that operate based on signals from an arbitration state machine 52, but Applicants could find no suggestion of associating a peripheral-share register with each of plurality of peripherals and then operating a multiplexor based on values in these registers. Starke shows a register file 305 within a processor 301 but no peripheral-share register associated with a peripheral such as memory 302 and certainly not a plurality of such registers that each reside at and are associated with particular peripherals. For these reasons, the combined teaching of Tanaka, Stirk, and Starks fail to support a rejection of the system of claim 1, and this rejection should be withdrawn.

Additionally, the peripheral-share registers are configured for sharing among the processors by including "an entry holding a state value indicating which of the plurality of processors currently owns the peripheral unit." As stated in Applicants' specification in the last sentence of para. [0029], the "sharing of peripheral control registers 203 is important because duplication of these registers would result in a need for duplicate sets of control registers at each peripheral unit 202 and the content of the registers 203 would have to be multiplexed based on peripheral ownership in order to control a peripheral unit 202." As a result, the claimed shared peripheral-share registers are more effective in allowing the multiplexer to use an owner signal based on the state value "such that only the one of the processors indicated as currently owning the peripheral is coupled by the multiplexor to the peripheral."

The Response to Arguments at page 14 states that "Tanaka teaches coupling each of the plurality of processors to the bus in response to an owner signal (Fig. 1 and col. 3, lines 44-64)." However, Tanaka in Fig. 1 and col. 3 does not teach that each of its shared registers, R1-R4, includes a state value for each of the processors, P1-P4, that indicates its ownership or lack of

ownership of a peripheral (or even of the memory register itself). Instead, in col. 3, lines 44-64, Tanaka teaches the use of separate storage areas M1-M4 that are used to indicate which processor P1-P4 is using which memory register R1-R4, which does not even suggest multiplexing of processors as called for in claim 1. In the Response to Arguments, Stirk is again only cited for teaching the use of a multiplexor, but Stirk fails to teach a register at each of a plurality of peripherals and a mulitplexor coupling processors by processing an ownership signal based on a state value at the registers associated the processor. For this additional reason, claim 1 is believed in condition for allowance over Tanaka, Stirk, and Starke.

For completeness and ease of the Examiner, the reasons for allowing claim 1 that were provided in the prior Amendment are still believed applicable and are provided:

> "Claim 1 further calls for a multiplexor for selectably coupling each of the plurality of processors to the bus in response to an owner signal. The Office Action states that Tanaka fails to teach such a multiplexor and cites Stirk at data MUX 46, address MUX 50, and associated circuits for teaching the multiplexor of claim 1. While Stirk shows the use of multiplexors, it fails to show coupling outputs of such processors to shared peripherals "in response to an owner signal" but instead apparently operates the data write MUX 46 and address MUX 50, at least in part, with an arbitration state machine 52, which is different than the use of an owner signal as called for in claim 1.
>
> .....Stirk fails to teach that its multiplexors are operated based on an owner signal and certainly, does not teach that the owner signal is based on the one of the state values in an entry of a state register associated with a peripheral unit. Tanaka does not overcome this deficiency with its "shared register control portion." The Office Action cites Starke for teaching an embedded system, but Starke fails to teach the control of a multiprocessor with an owner control signal or basing the owner signal on a state value indicating ownership of a peripheral unit. Because the

combination of the three references fails to teach or suggest each element of claim 1, the rejection is improper and should be withdrawn."

As noted in the prior Amendment, Claims 2, 5, 7, and 8 depend from claim 1 and are believed allowable as depending from an allowable base claim. The Response to Arguments failed to address the following addition reason for allowing claims 5 and 8, and Applicants request that these arguments be fully considered by the Examiner and a response be provided:

> "... claim 5 calls for the set of peripheral share registers to include release registers corresponding to the processors and having an entry associated with each one of the peripheral units to hold a value indicating whether the processor is releasing ownership. The Office Action cites Tanaka for teaching this limitation with elements M1 through M4. However, these are storage areas that are described at col. 3, lines 65-68 as corresponding to the processors. There is no teaching that in the storage area an entry holding a value is stored that indicates whether one of the processor is releasing one or more peripheral devices or units. Claim 8 calls for one of the processors to be able to dynamically alter the state value used to generate the owner signal. Tanaka is cited at col. 4, lines 33-66 for teaching this element but at this citation, Tanaka is merely discussing accessing shared registers R1-R4 with processors P1-P4 and is not teaching a processor altering state values that control which of the processors can access peripheral units. For these additional reasons, claims 5 and 8 are believed allowable over the combined teaching of the references."

Independent claim 25 is a system provided in a single integrated circuit that includes peripheral units and within the same integrated circuit a peripheral register associated with each of the peripheral units. Within each register is provided a state value associated with each of the processors. A multiplexor performs coupling of the processors to a peripheral bus based on these state values. The Response to Arguments states that Tanaka and Stirk teach the operation of the multiplexor of claim 25. Applicant disagrees because these

references fail to show a register with a state value for each processor and the register is associated with a particular peripheral. The references also fail to show a multiplexor that couples processors to a peripheral bus based on values of these state values. Hence, the references fail to support a rejection of claim 25 under 35 U.S.C. §103 because the references fail to show or suggest each and every element of claim 25.

Claims 27-28 depend from claim 25 and are believed allowable for the reasons provided for allowing claim 25. Claim 27 is believed allowable for the reasons provided for allowing claim 10. Claim 28 further defines the multiplexor and indicates how the portions are operated according to the state of the owner signal, which is not shown by the references. For these additional reasons, the rejection of claims 26-28 based on Tanaka, Stirk, and Starke is improper, and Applicants respectfully request that this rejection be withdrawn.

Rejection under 35 U.S.C. 103 of Claims 3 and 30

Claims 3 and 30 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Stirk and Starke further in view of U.S. Pat. No. 6,480,952 ("Gorishek"). This rejection is respectfully traversed based on the following remarks.

Claims 3 and 30 depend from claims 1 and 25, respectively, and are believed allowable as depending from an allowable base claim. Particularly, Gorishek fails to overcome the deficiencies noted for Tanaka, Stirk, and Starke with reference to claims 1 and 25, e.g., Gorishek fails to teach a multiplexor that couples processors to a peripheral bus based on an owner signal.

Rejection under 35 U.S.C. 103 of Claims 4 and 29

In the Office Action, claims 4 and 29 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Stirk and Stark further in view of U.S. Pat. No. 5,317,749 ("Dahlen"). This rejection is respectfully traversed based on the following remarks.

Claims 4 and 29 depend from claims 1 and 25, respectively, and are believed allowable as depending from an allowable base claim. Particularly,

Dahlen fails to overcome the deficiencies noted for Tanaka, Stirk, and Starke with reference to claims 1 and 25. Dahlen fails to teach a multiplexor that couples processors to a peripheral bus based on an owner signal.

Rejection under 35 U.S.C. 103 of Claim 6

In the Office Action, claim 6 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Stirk and Stark further in view of U.S. Pat. No. 5,678,026 ("Vartti"). This rejection is respectfully traversed based on the following remarks.

Claim 6 depends from claim 1 and is believed allowable as depending from an allowable base claim. Further, Vartti fails to overcome the deficiencies noted for Tanaka, Stirk, and Starke with reference to claim 1.

Rejection under 35 U.S.C. 103 of Claims 9-12

In the Office Action, claims 9-12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Dahlen in view of U.S. Pat. No. 5,317,749 ("Lehman"). Claims 9-12 are canceled.

Rejection under 35 U.S.C. 103 of Claims 13-19

In the Office Action, claims 13-19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Stirk and Starke further in view of Lehman. This rejection is respectfully traversed based on the following remarks.

Claim 13 is directed to a multiprocessor controller with limitations similar to claim 1, and hence, claim 13 is believed allowable over Tanaka, Stirk, and Starke for the reasons provided for allowing claim 1. Lehman does not overcome the deficiencies of these three references. Claim 14-16, 18, and 19 depend from claim 13 and are believed allowable as depending from an allowable base claim.

Conclusions

In view of all of the above, the claims are now believed to be allowable and the case in condition for allowance which action is respectfully requested.

No fees are believed due with this Amendment. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

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